



# ACTT6B-800E

## AC Thyristor Triac power switch

27 February 2013

Product data sheet

### 1. General description

AC Thyristor Triac power switch in a SOT404 (D2PAK) surface mountable plastic package with self-protective clamping capabilities against low and high energy transients.

### 2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- Direct interfacing with low power drivers and microcontrollers
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Sensitive gate for easy logic level triggering
- Surface mountable package
- Triggering in three quadrants only
- Very high immunity to false turn-on by  $dV/dt$

### 3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls

### 4. Quick reference data

Table 1. Quick reference data

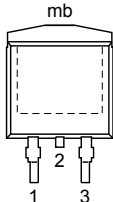
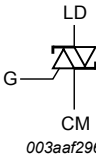
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	-	800	V
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	51	A
$T_j$	junction temperature		-	-	125	$^{\circ}\text{C}$
$I_{T(\text{RMS})}$	RMS on-state current	full sine wave; $T_{mb} \leq 108\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	6	A



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>PP</sub>	peak pulse voltage	T <sub>j</sub> = 25 °C; non-repetitive, off-state; <a href="#">Fig. 6</a>	-	-	2	kV
<b>Static characteristics</b>						
I <sub>GT</sub>	gate trigger current	V <sub>D</sub> = 12 V; I <sub>T</sub> = 100 mA; LD+ G+; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>	-	-	10	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 100 mA; LD+ G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>	-	-	10	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 100 mA; LD- G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>	-	-	10	mA
V <sub>CL</sub>	clamping voltage	I <sub>CL</sub> = 0.1 mA; t <sub>p</sub> = 1 ms; T <sub>j</sub> = 25 °C	850	-	-	V
<b>Dynamic characteristics</b>						
dV <sub>D</sub> /dt	rate of rise of off-state voltage	V <sub>DM</sub> = 536 V; T <sub>j</sub> = 125 °C; (V <sub>DM</sub> = 67% of V <sub>DRM</sub> ); exponential waveform; gate open circuit; <a href="#">Fig. 13</a>	500	-	-	V/μs
di <sub>com</sub> /dt	rate of change of commutating current	V <sub>D</sub> = 400 V; T <sub>j</sub> = 125 °C; I <sub>T(RMS)</sub> = 6 A; dV <sub>com</sub> /dt = 1 V/μs; gate open circuit; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	10	-	-	A/ms

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 <p style="text-align: center;"><b>D2PAK (SOT404)</b></p>	 <p style="text-align: center;">003aaf296</p>
2	LD	load		
3	G	gate		
mb	LD	mounting base; load		

## 6. Ordering information

Table 3. Ordering information

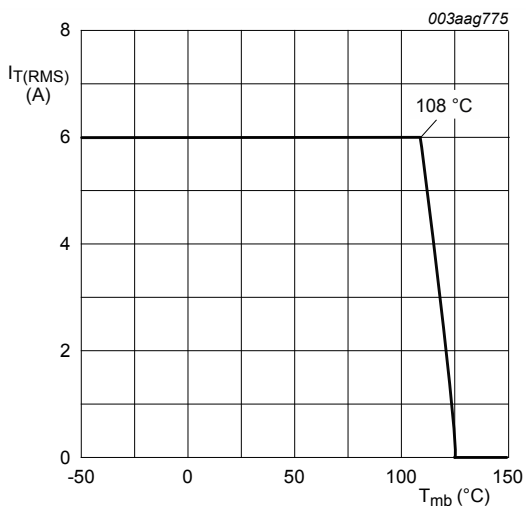
Type number	Package		Version
	Name	Description	
ACTT6B-800E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 7. Limiting values

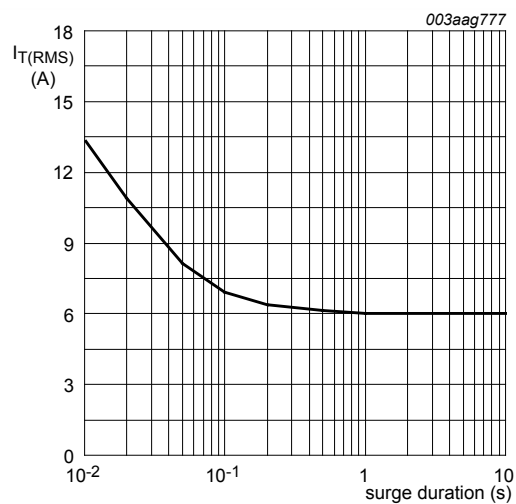
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 108\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	6	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 16.7\text{ ms}$	-	56	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	51	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; sine-wave pulse	-	13	$\text{A}^2\text{s}$
$di_T/dt$	rate of rise of on-state current	$I_T = 9\text{ A}$ ; $I_G = 0.2\text{ A}$ ; $di_G/dt = 0.2\text{ A}/\mu\text{s}$	-	100	$\text{A}/\mu\text{s}$
$I_{GM}$	peak gate current	$t = 20\text{ }\mu\text{s}$	-	2	A
$P_{GM}$	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
$T_{stg}$	storage temperature		-40	150	$^{\circ}\text{C}$
$T_j$	junction temperature		-	125	$^{\circ}\text{C}$
$V_{PP}$	peak pulse voltage	$T_j = 25\text{ }^{\circ}\text{C}$ ; non-repetitive, off-state; <a href="#">Fig. 6</a>	-	2	kV



**Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values**



**Fig. 2. RMS on-state current as a function of surge duration; maximum values**

$f = 50\text{ Hz}$ ;  $T_{mb} = 108\text{ }^{\circ}\text{C}$

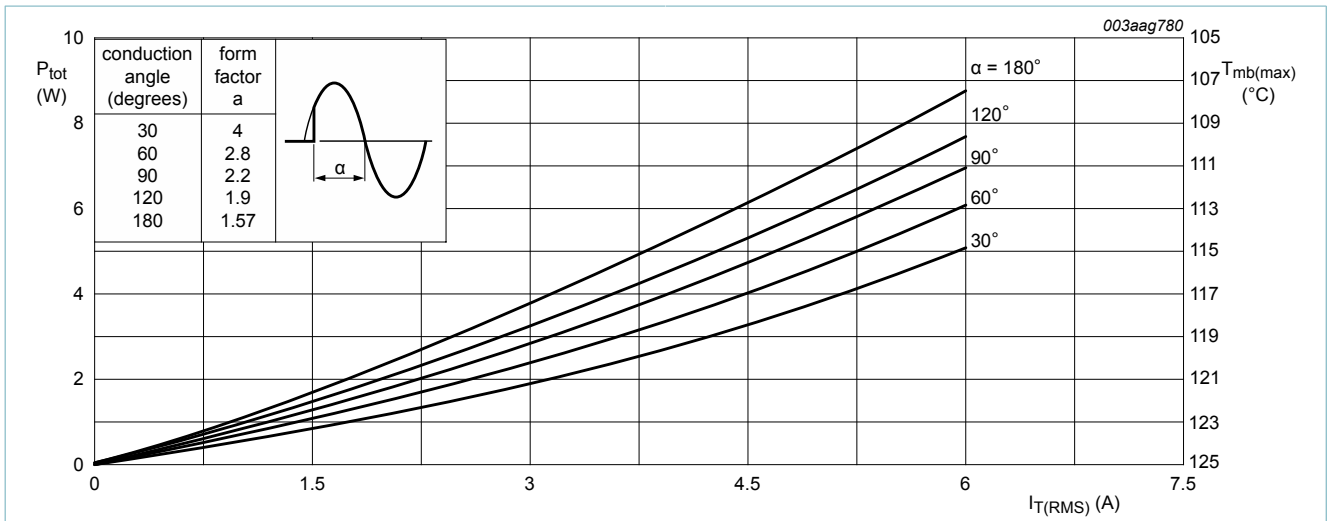


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

$\alpha =$  conduction angle  
 $a =$  form factor =  $I_{T(RMS)} / I_{T(AV)}$

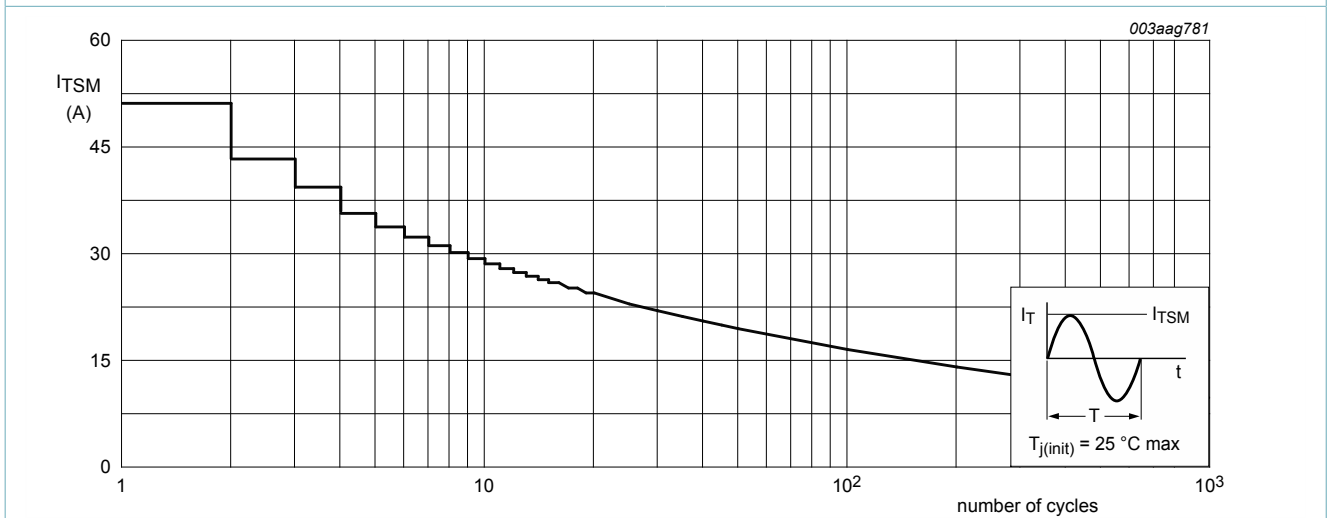


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

$f = 50\text{ Hz}$

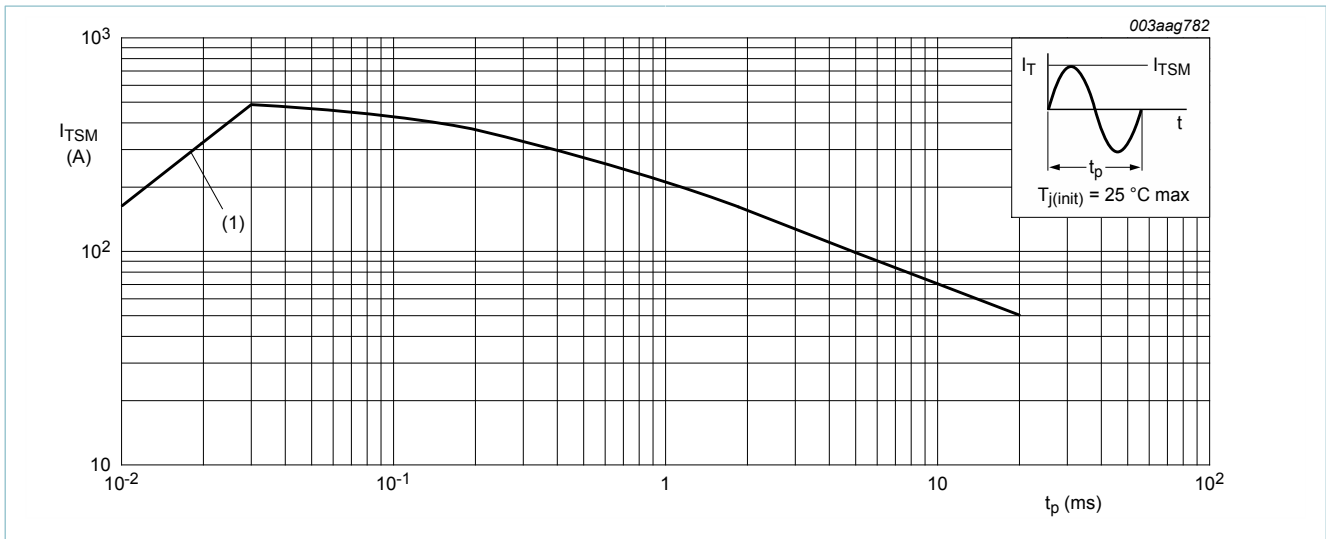


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

$t_p \leq 20 \text{ ms}$ ; (1)  $dI_T/dt$  limit

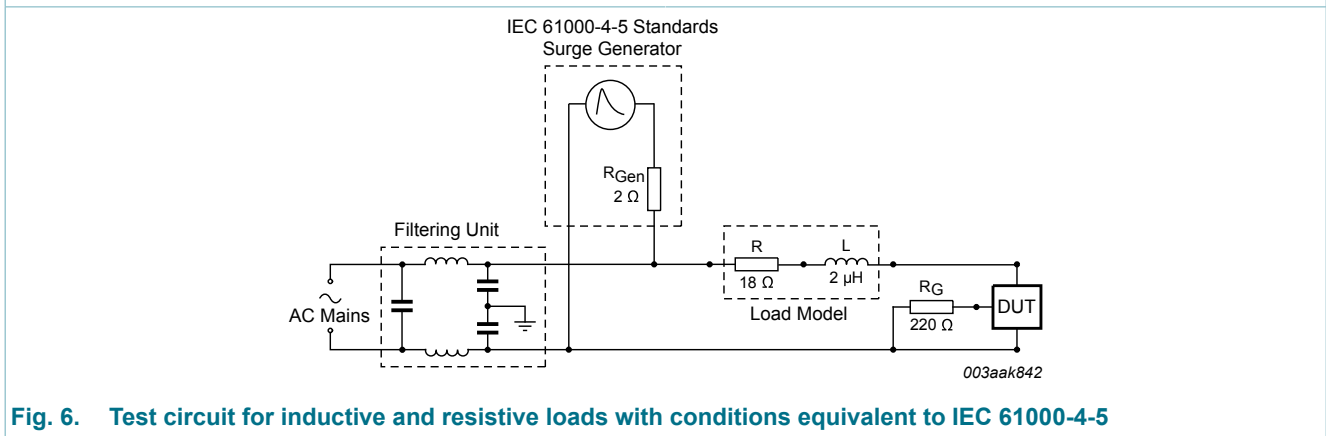
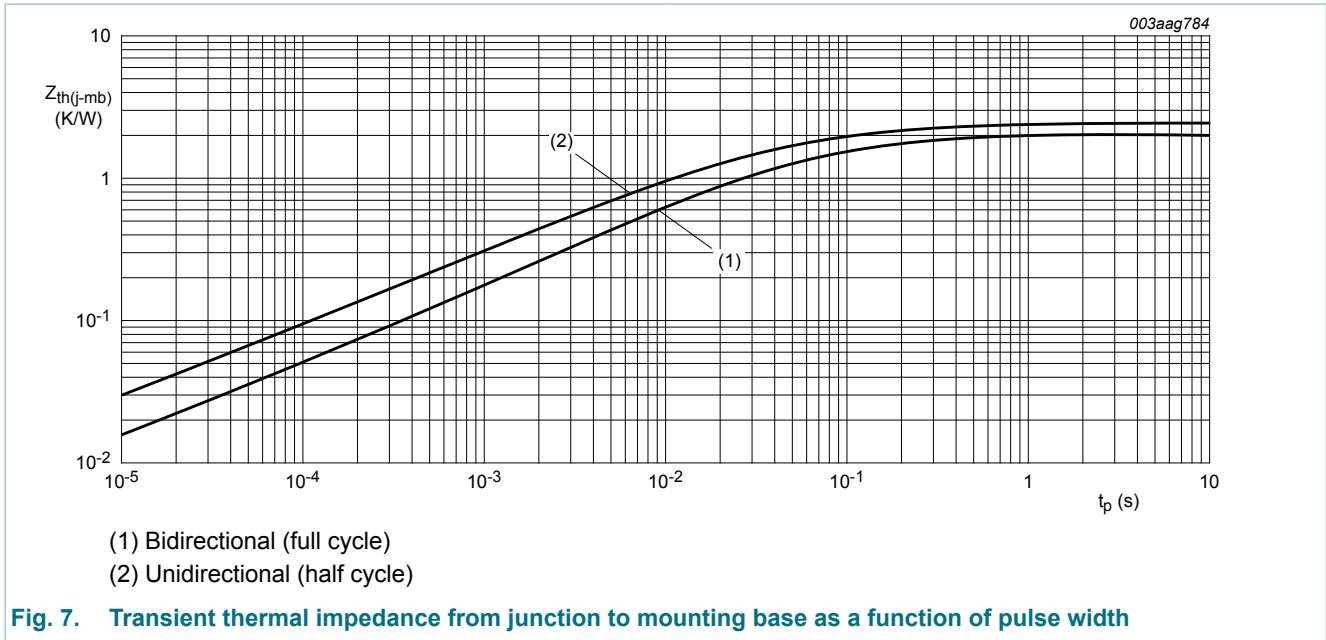


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

## 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	half cycle; <a href="#">Fig. 7</a>	-	-	2.4	K/W
		full cycle; <a href="#">Fig. 7</a>	-	-	2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed circuit board (FR4) mounted	-	55	-	K/W

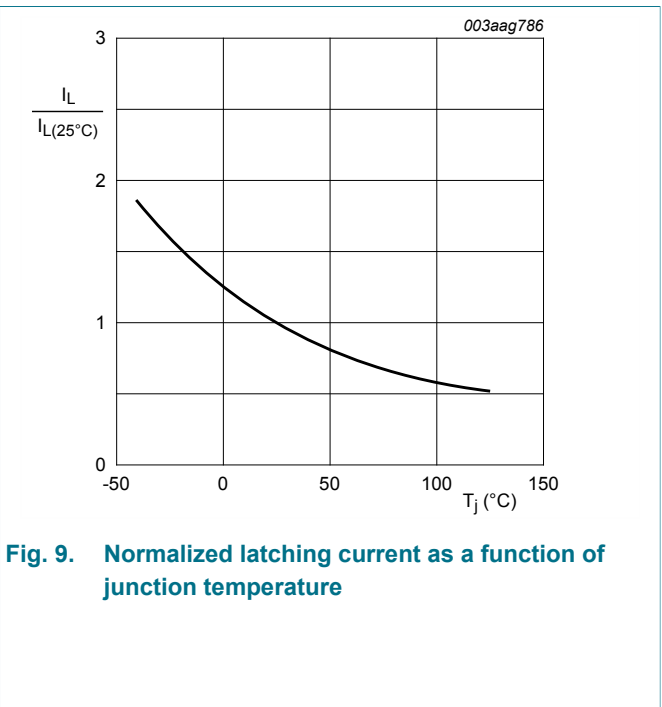
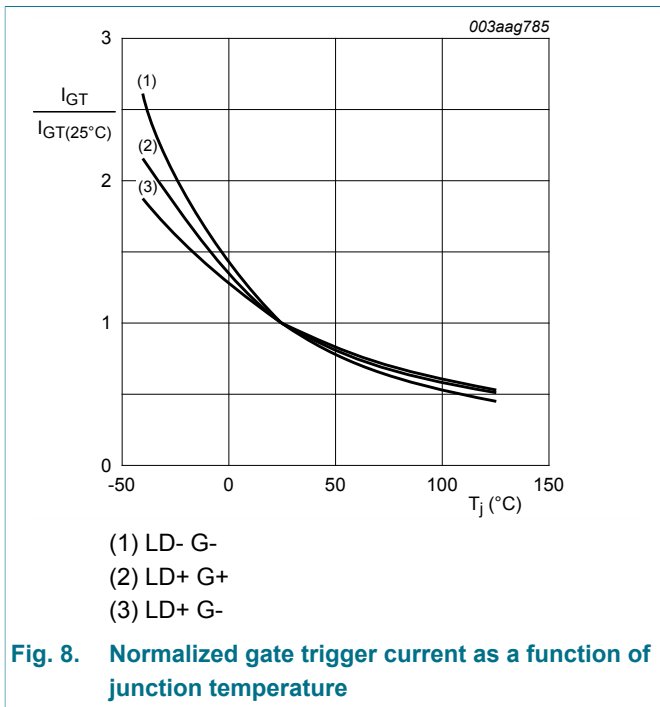


## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}; I_T = 100\text{ mA}; LD+ G+;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	10	mA
		$V_D = 12\text{ V}; I_T = 100\text{ mA}; LD+ G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	10	mA
		$V_D = 12\text{ V}; I_T = 100\text{ mA}; LD- G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	10	mA
$I_L$	latching current	$V_D = 12\text{ V}; I_G = 100\text{ mA}; LD+ G+;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 9	-	-	30	mA
		$V_D = 12\text{ V}; I_G = 100\text{ mA}; LD+ G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 9	-	-	40	mA
		$V_D = 12\text{ V}; I_G = 100\text{ mA}; LD- G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 9	-	-	30	mA
$I_H$	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 10	-	-	25	mA
$V_T$	on-state voltage	$I_T = 8\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 11	-	-	1.7	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}; I_T = 100\text{ mA}; T_j = 25\text{ }^\circ\text{C};$ Fig. 12	-	0.8	1	V
		$V_D = 400\text{ V}; I_T = 100\text{ mA}; T_j = 125\text{ }^\circ\text{C};$ Fig. 12	0.2	0.45	-	V
$I_D$	off-state current	$V_D = 800\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	-	10	$\mu\text{A}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 800\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	-	0.5	mA
$V_{CL}$	clamping voltage	$I_{CL} = 0.1\text{ mA}; t_p = 1\text{ ms}; T_j = 25\text{ }^\circ\text{C}$	850	-	-	V
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_j = 125\text{ }^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM});$ exponential waveform; gate open circuit; <a href="#">Fig. 13</a>	500	-	-	V/ $\mu\text{s}$
$dI_{com}/dt$	rate of change of commutating current	$V_D = 400\text{ V}; T_j = 125\text{ }^\circ\text{C}; I_{T(RMS)} = 6\text{ A};$ $dV_{com}/dt = 20\text{ V}/\mu\text{s};$ (snubberless condition); gate open circuit; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	3.5	-	-	A/ms
		$V_D = 400\text{ V}; T_j = 125\text{ }^\circ\text{C}; I_{T(RMS)} = 6\text{ A};$ $dV_{com}/dt = 10\text{ V}/\mu\text{s};$ gate open circuit; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	5	-	-	A/ms
		$V_D = 400\text{ V}; T_j = 125\text{ }^\circ\text{C}; I_{T(RMS)} = 6\text{ A};$ $dV_{com}/dt = 1\text{ V}/\mu\text{s};$ gate open circuit; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	10	-	-	A/ms



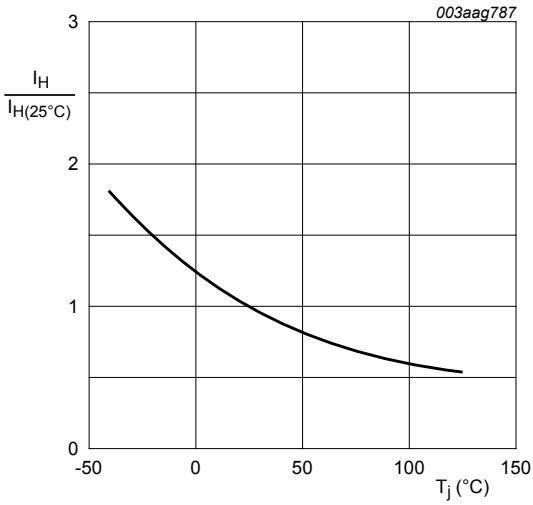
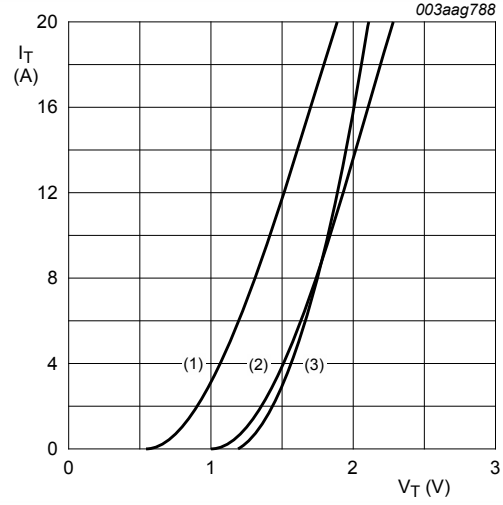


Fig. 10. Normalized holding current as a function of junction temperature



$V_o = 1.109 \text{ V}; R_s = 0.076 \Omega$

- (1)  $T_j = 125^\circ\text{C}$ ; typical values
- (2)  $T_j = 125^\circ\text{C}$ ; maximum values
- (3)  $T_j = 25^\circ\text{C}$ ; maximum values

Fig. 11. On-state current as a function of on-state voltage

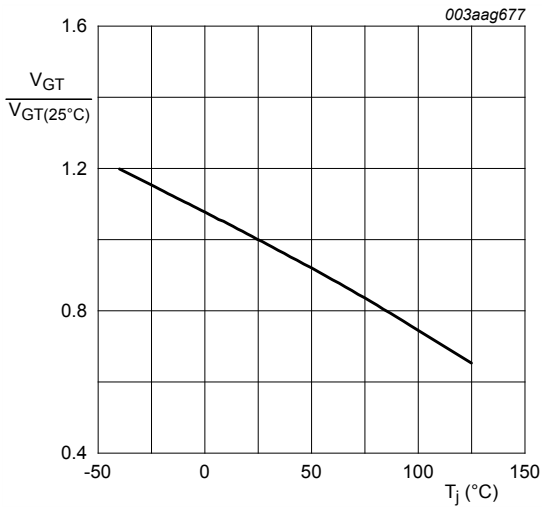
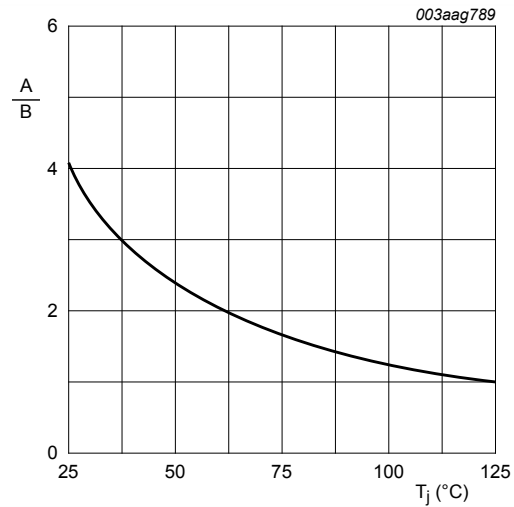


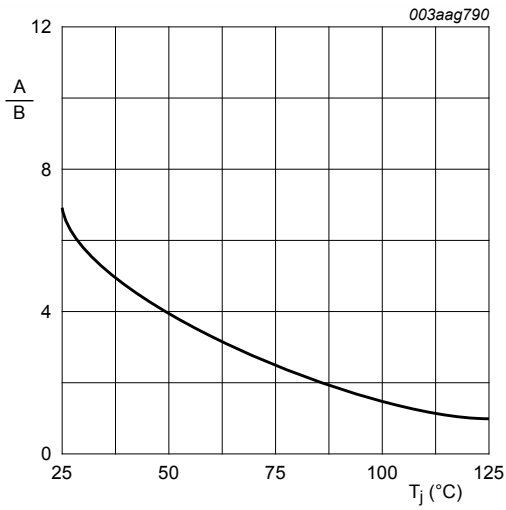
Fig. 12. Normalized gate trigger voltage as a function of junction temperature



A is  $dV_D/dt$  at condition  $T_j$  °C  
 B is  $dV_D/dt$  at condition  $T_j$  125 °C

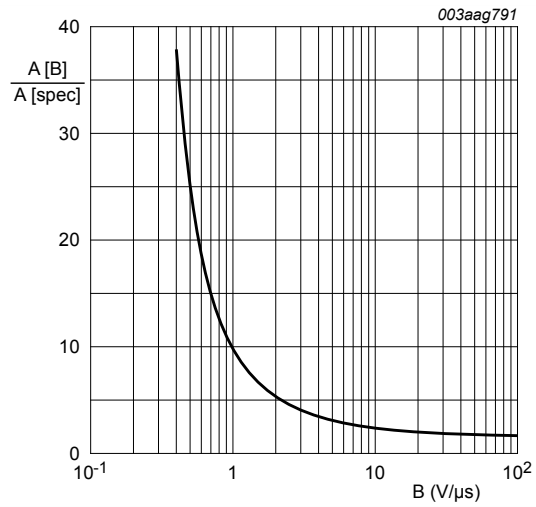
Fig. 13. Normalized rate of rise of off-state voltage as a function of junction temperature





A is  $di_{com}/dt$  at condition  $T_j$  °C  
 B is  $di_{com}/dt$  at condition  $T_j$  125 °C  
 $V_D = 400$  V

**Fig. 14. Normalized critical rate of rise of commutating current as a function of junction temperature**

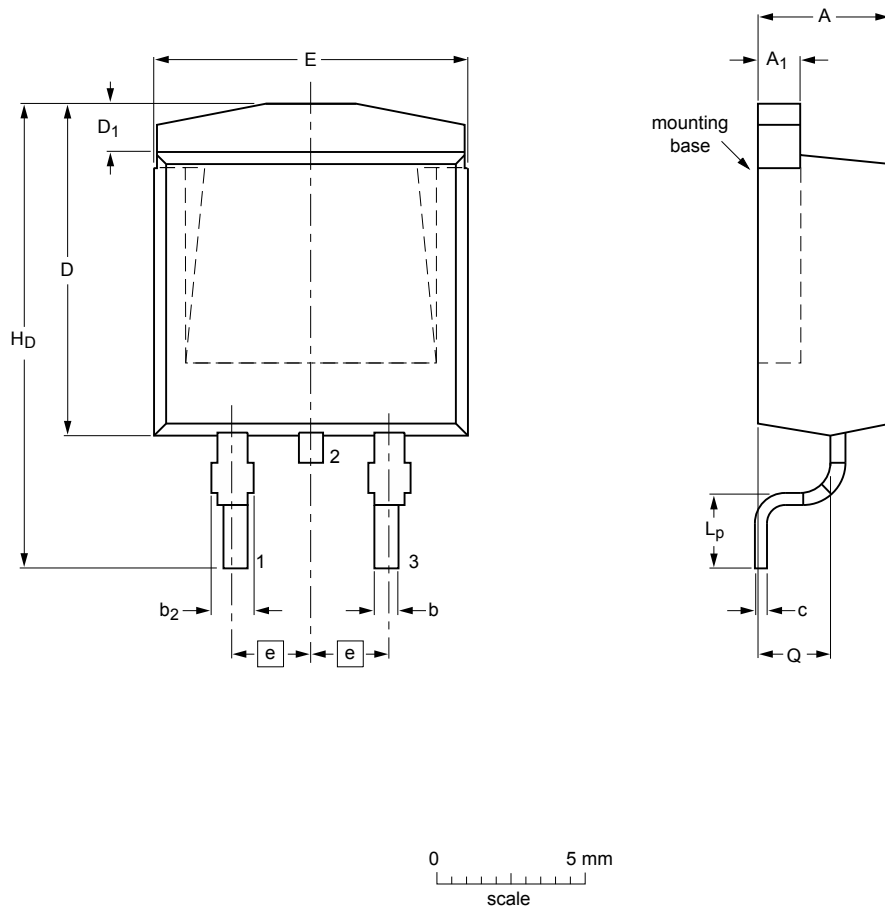


A[B] is  $di_{com}/dt$  at condition B,  $dV_{com}/dt$   
 A[spec] is the specified data sheet value of  $di_{com}/dt$   
 turn-off time < 20 ms

**Fig. 15. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values**

### 10. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	b	b <sub>2</sub>	c	D	D <sub>1</sub>	E	e	H <sub>D</sub>	L <sub>p</sub>	Q
max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
nom									2.54			
min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT404					-06-03-16- 13-02-25

Fig. 16. Package outline D2PAK (SOT404)

### 11. Soldering

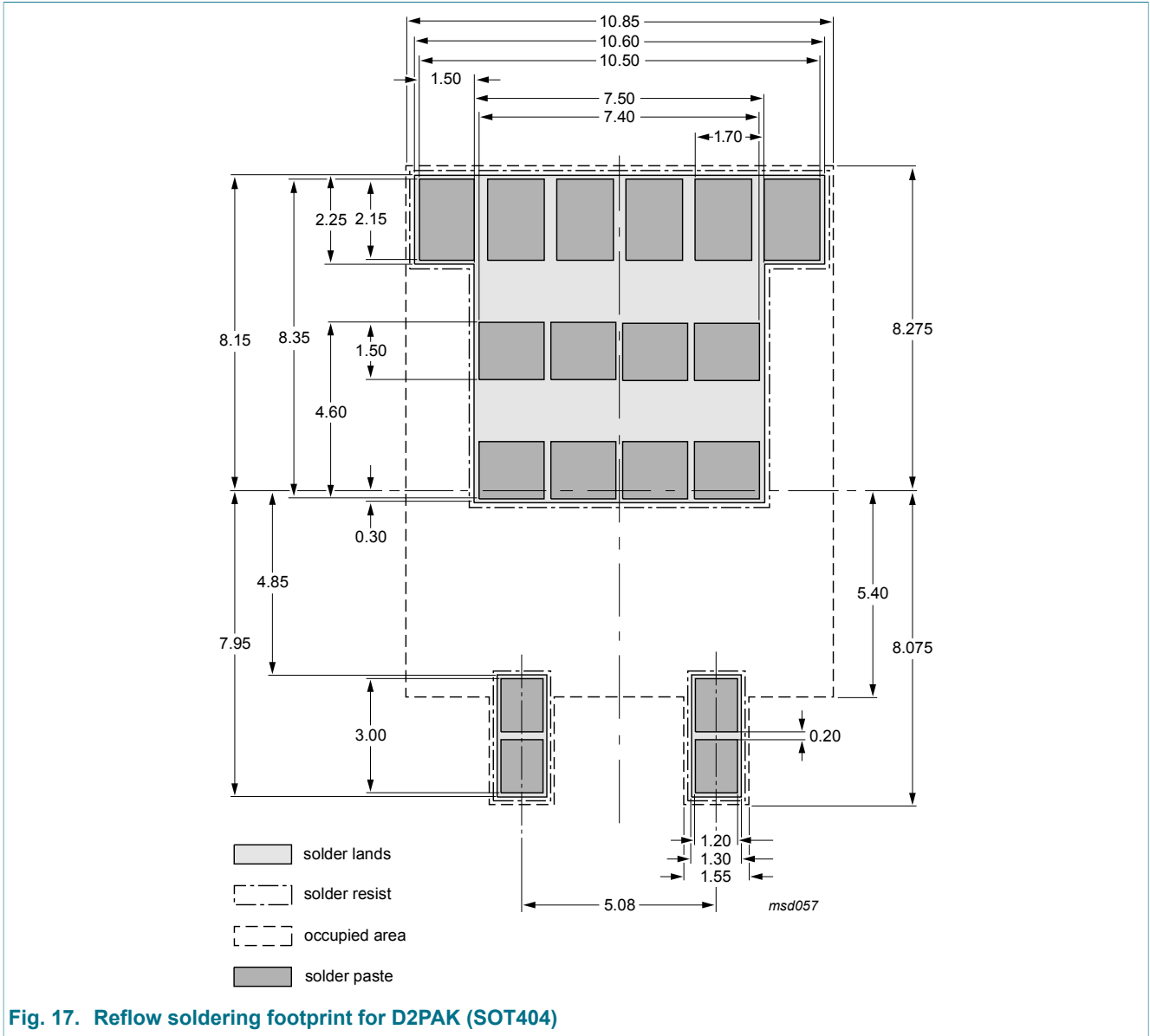


Fig. 17. Reflow soldering footprint for D2PAK (SOT404)

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Document status [1][2]	Product status [3]	Definition
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